REMARKS

Claim 3 is pending in the present application. In light of the Office Action mailed January 12, 2006, claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application No. 10/280,974, Publication No. 2004/0082094 ("Yamamoto") in view of US Patent Application No. 09/836,160, Publication No. 2002/0148946 ("Tu"). The applicant respectfully disagrees with this rejection.

The combination of Yamamoto and Tu does not teach or suggest all of the elements of claim 3 in the present application. The Examiner maintains that Yamamoto teaches the features of claim 3 except that Yamamoto is silent about using a ball grid array (BGA) on the underside of the die. The Examiner suggests that Tu discloses a structure of an image sensor having at least an image sensing chip overlying a BGA. The Examiner goes on to suggest that it would have been obvious to modify the image sensor die of Yamamoto with a BGA on the underside of the image sensor die for the purpose of electrically connecting the Yamamoto image sensor to a printed circuit board. Additionally, the Examiner suggests that "the BGA type semiconductor device [in Tu] can be used as an image sensor chip" and "[t]herefore, in *Tu et al* '946 the stacked structure of the image sensor must be the image sensor die having balls 30 on its underside." The undersigned disagrees because the combination of Yamamoto and Tu does not teach or suggest, *inter alia*, an image sensor die that uses a ball grid array (BGA) **on** the underside of the die.

Claim 3 of the present application is directed toward a method that includes forming a plurality of image sensor die having micro-lenses onto a semiconductor wafer. The image sensor die uses a ball grid array (BGA) on the underside of the die. The method further includes forming a protective layer over said image sensor die, dicing the wafer to separate the plurality of image sensor die, and mounting the image sensor die onto an integrated circuit package. The method still further includes removing the protective layer from the image sensor die.

Yamamoto discloses an image sensor die having contact pads on top of the die next to the pixels and the protective layer covering the pixels (Paragraphs e 29-32; Figure 5). The contact pads of the image sensor die in Yamamoto are configured to be connected to pins of an integrated circuit package (lead frame) via bonding wires (paragraphs 29-33; Figure 6).

Yamamoto does not teach or suggest using a BGA to connect the image sensor die to the rest of the integrated circuit package.

Tu discloses a stacked structure of an image sensor or an image sensor package having an image sensor chip or die 16 arranged on a package layer 14 so as to from a stacked structure with an integrated circuit 12 (paragraphs 6, 13 and 19; Figure 1). The integrated circuit 12 is a digital signal processor, a microprocessor, or a central processing unit (paragraph 21). The integrated circuit 12 is electrically connected to signal input terminals 28 on an upper surface 24 of a substrate 10 via wires 22 (paragraphs 20-21; Figure 1). A package layer 14 covers the integrated circuit and provides protection to the integrated circuit 12 and the associated wires 22 (paragraph 22). The image sensor die 16 is positioned on top of the package layer 14 and contacts on top of the image sensor die 16 are connected to input terminals 28 on the top surface 24 of the substrate 10 of the image sensor package via wires 22 (paragraphs 20 and 23; Figure 1-6). The substrate 10 includes output terminals 30 formed on a lower surface 26 of the substrate 10 (paragraph 20; Figure 1). The output terminals 30 on the lower surface 26 of the substrate 10 can be used to connect the substrate 10 of the image sensor package to a printed circuit board using a ball grid array (paragraph 20; Figures 1-6). It is important to note that Figures 2 and 3 show the integrated circuit 12, the substrate 10, and the output terminals 30 of Tu without the image sensor die 16.

Although Tu does disclose using a ball grid array to connect the image sensor package to a printed circuit board, Tu does not teach or suggest using a ball grid array on the underside of the image sensing die to connect the image sensing die to the rest of the image sensor package.

The combination of Yamamoto and Tu does not teach or suggest, *inter alia*, an image sensor die that uses a ball grid array (BGA) **on** the underside of the die, as recited in claim 3. As discussed and shown in the present application, a BGA arrangement allows contacts on the image sensor die to be electrically connected to contacts on an integrated circuit package without the need to expose any of the top surface of the image sensor wafer or the need for bonding wires (para. 19; Figures 2-5). In Yamamoto, wires are used to connect contact pads on top of an image sensor die to pins of an integrated circuit package (lead frame). The lead frame can then be connected to a printed circuit board.

Tu discloses connecting bond pads on top of an image sensor die to input terminals on a substrate of an integrated circuit package via wires. The substrate of the image sensor package can then be connected to a printed circuit board via a ball grid array. Tu does not teach or suggest using any type of contacts or connectors **on** the underside of the die. In Tu, the integrated circuit package has a ball grid array attached to the underside of the package, but there is no ball grid array used **on** the underside of the image sensor die.

In Tu, the underside of the image sensing die is positioned against a packaging layer. In fact, in Tu, the packaging layer appears to cover the entire underside of the image sensing die. The packaging layer is positioned on top of an integrated circuit, which is positioned on top of a substrate (Figures 4-6). The ball grid array in Tu is **on** the underside of the substrate. The image sensing die in Tu is electrically connected to the substrate via wires that connect to the top of the image sensing die. Accordingly, even if the image sensing die in Tu overlies the ball grid array, the ball grid array in Tu is **not physically on the underside** of the image sensing die and **not electrically connected to the underside** of the image sensing die. Accordingly, the image sensing die in Tu does not use a ball grid array on the underside of the die.

Additionally, in Tu, the image sensor package includes or contains the image sensor die. Accordingly, the image sensor package cannot be the image sensor die as suggested by the Examiner.

Both references disclose connecting contacts on the top of an image sensor to other portions of an integrated circuit package using wires. Neither reference discloses contacts of any kind on the underside of an image sensor die, let a lone an image sensor die that uses a ball grid array (BGA) <u>on</u> the underside of the die, as recited in claim 3 of the present application.

Furthermore, combining Yamamoto with Tu does not teach or suggest an image sensor die that uses a ball grid array (BGA) on the underside of the die. If the packaging of Tu were combined with image sensor die of Yamamoto, the result would be the contacts on the top of the image sensor die of Yamamoto connected to the substrate of Tu via wires. The substrate in Tu could then be used to connect the integrated circuit package (image sensor package) to a printed circuit board via a ball grid array. There is no suggestion of using a ball grid array **<u>on</u>** the underside of the image sensor die in either reference. Accordingly, one skilled in the art could only arrive at the claimed subject matter by using the present application and applying impermissible hindsight. Therefore, the combination of Tu and Yamamoto fails to teach or suggest an image sensor die that uses a ball grid array (BGA) **<u>on</u>** the underside of an image sensor die.

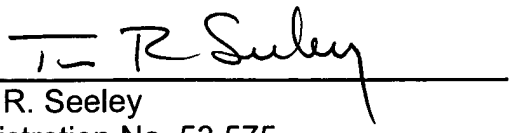
For at least these reasons, claim 3 is in condition for allowance.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 50-0665, under Order No. 384938073US from which the undersigned is authorized to draw.

Respectfully submitted,
Perkins Coie LLP

Date: March 13, 2006



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